Notice of Allowability	Application No.	Applicant(s)	
	09/592,572	DELLACONA, RICHARD	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *29 January 2007*.

2. ☒ The allowed claim(s) is/are *1-3,5-13,16-21,23-31 and 34-37*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Introduction

1. This communication is in response to the Applicants' communication dated January 29, 2007. Claims 1 and 19 were amended. Claim 37 was added. Claims 1-3, 5-13, 16-21, 23-31 and 34-37 of the application are pending.

Examiner's Amendment

2. Authorization for this examiner's amendment was given in a telephone conversation by Mr. David Parkhurst on April 12, 2007.

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to the applicants, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3. In the claims:

Amended claim 1, Lines 12-24, "(b) a storage device bypass circuit board associated with each storage device, each storage device being plugged into a connector on the storage device bypass circuit board, and each of said storage device bypass circuit boards of said first and

second mass storage modules including first and second electrical switches, each of said first and second electrical switches including input and output electrical connections to said first and second controllers, respectively, each of said first and second electrical switches including input and output electrical connections to a corresponding one of said plug-in storage devices, and a fault signal output produced by said corresponding one of said plurality of storage devices being connected to each of said first and second electronic switches to control switching of said first and second electrical switches to alternatively route signals to and from said first and second controllers to and from said corresponding one of said plurality of storage devices, or to bypass said corresponding one of said plurality of storage devices;"

has been changed to

-- (b) a storage device bypass circuit board associated with each storage device, each storage device being plugged into a connector on the storage device bypass circuit board, and each of said storage device bypass circuit boards of said first and second mass storage modules including first and second electronic switches, each of said first and second electronic switches including input and output electrical connections to said first and second controllers, respectively, each of said first and second electronic switches including input and output electrical connections to a corresponding one of said plug-in storage devices, and a fault signal output produced by said corresponding one of said plurality of storage devices being connected to each of said first and second electronic switches to control switching of said first and second electronic switches to alternatively route signals from and to said first and second controllers to and from said corresponding one of said plurality of storage devices, or to bypass said corresponding one of said plurality of storage devices;--.

Amended claim 19 Lines 12-41, "(b) a disk drive bypass circuit board associated with each disk drive and including a disk drive connector at one edge thereof and a bypass board connector at another edge thereof, each disk drive being plugged into said disk drive connector on the disk drive bypass circuit board, each of said disk drive bypass circuit boards of said first and second, mass storage modules including first and second electrical switches, each of said first and second electrical switches including input and output electrical connections to said first and second controllers, respectively, each of said first and second electrical switches including input and output electrical connections to a corresponding one of said plug-in disk drives, and a fault signal output produced by said corresponding one of said plurality, of disk drives being connected to each of said first and second electronic switches to, control switching of said first and second electrical switches to alternatively route signals to and from said first and second controllers to and from said corresponding one of said plurality of storage devices, or to bypass said corresponding one of said plurality of storage devices,;

(c) a module bypass circuit board including an optical input/output connector for outputting electrical signals from the module as light signals and for inputting light signals into the module as electrical signals, and wherein the optical input/output connectors of the module bypass circuit boards of the first and second mass storage modules are connected by a fiber optic transmission medium such that signals are communicated between the modules in the form of light, each of said module bypass circuit boards of said first and second mass storage modules including first and second electrical switches, each of said first and second electrical switches including input and output electrical connections to said first and second

controllers, respectively, each of said first and second electrical switches including input and output electrical connections to said optical input/output connector, and a signal detect output produced by said optical input/output connector being connected to each of said first and second electronic switches to control switching of said first and second electrical switches to alternatively route signals to and from said first and second controllers to and from a corresponding one of said first and second mass storage modules, or to bypass said corresponding one of said first and second mass storage modules;"

has been changed to

-- (b) a disk drive bypass circuit board associated with each disk drive and including a disk drive connector at one edge thereof and a bypass board connector at another edge thereof, each disk drive being plugged into said disk drive connector on the disk drive bypass circuit board, each of said disk drive bypass circuit boards of said first and second mass storage modules including first and second electronic switches, each of said first and second electronic switches including input and output electrical connections to said first and second controllers, respectively, each of said first and second electronic switches including input and output electrical connections to a corresponding one of said plug-in disk drives, and a fault signal output produced by said corresponding one of said plurality of disk drives being connected to each of said first and second electronic switches to control switching of said first and second electronic switches to alternatively route signals from and to said first and second controllers to and from said corresponding one of said plurality of disk drives, or to bypass said corresponding one of said plurality of disk drives;

(c) a module bypass circuit board including an optical input/output connector for outputting electrical signals from the module as light signals and for inputting light signals into the module as electrical signals, and wherein the optical input/output connectors of the module bypass circuit boards of the first and second mass storage modules are connected by a fiber optic transmission medium such that signals are communicated between the modules in the form of light, each of said module bypass circuit boards of said first and second mass storage modules including first and second electronic switches, each of said first and second electronic switches including input and output electrical connections to said first and second controllers, respectively, each of said first and second electronic switches including input and output electrical connections to said optical input/output connector, and a signal detect output produced by said optical input/output connector being connected to each of said first and second electronic switches to control switching of said first and second electronic switches to alternatively route signals from and to said first and second controllers to and from a corresponding one of said first and second mass storage modules, or to bypass said corresponding one of said first and second mass storage modules;--.

Replace claim 37 with:

37. The high speed mass storage system of claim 1 wherein each of said module bypass circuit boards of said first and second mass storage modules include first and second electronic switches, each of said first and second electronic switches including input and output electrical connections to said first and second controllers, each of said first and second electronic switches including input and output electrical connections to said optical input/output connector,

and a signal detect output produced by said optical input/output connector being connected to each of said first and second electronic switches to control switching of said first and second electronic switches to alternatively route signals from and to said first and second controllers to and from a corresponding one of said first and second mass storage modules, or to bypass said corresponding one of said first and second mass storage modules.

Reasons for Allowance

4.. Claims 1-3, 5-13, 16-21, 23-31 and 34-37 of the application are allowed over prior art of record.

5. The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The closest prior art of record shows:

(1) a data storage system wherein each one of the disk interfaces is coupled to a corresponding disk drive; the disk interfaces in one portion are coupled through a first unidirectional channel to a first disk controller and the disk interfaces in another portion of the disk interfaces are coupled through a second unidirectional channel to a second disk controller; each disk interface includes a switch adapted to allow data to pass to another disk drive in the channel; when the other channel becomes inoperative, coupling the disk drive in the inoperative channel to the operative fibre channel; with such arrangement, a disk drive may be removed without requiring a shut-down of the storage system (i.e., the disk drive may be hot swapped); a

loop resiliency circuit switch is used to remove the inoperative disk from its channel; in one embodiment, a pair of switches is provided on the common printed circuit board with the disk interface for enabling removal of disk drives from the storage system (**Leshem,** U.S. Patent 5,729,763);

(2) a structure and method to provide communication loop resiliency for by-passing a failed controller in a dual active mode fibre channel loop of a dual ported disk storage system; the system has two active controllers each operable to control one or more controlled devices; the failed controller is bypassed by a loop resiliency circuit, which detects the failed controller on the basis of its output signal and selectively routes the signal received by the failed controller from the next downstream device on the loop to the output of the controller, so that next upstream device can continue operation on the fibre channel loop; the device bypass circuit (loop resiliency circuit) has a signal detection unit for detecting a valid first device signal and generating a first state signal and detecting a no valid first device signal and generating a second state signal; the loop resiliency circuits are provided between each controller and the controlled device for by-passing a failed controller (**El-Batal,** U. S. Patent 6,192,027);

(3) dynamically adding disk array chassis to an already operating disk drive array and communicating with the new disk array chassis before the disk drives are interfaced with the disk dive controller; the disk drives and a disk controller are connected in a loop with a first serial bus for transmitting data from the controller and a second serial bus for passing data back to the controller; the disk drives are connected to one or the other of serial busses; a shunt is connected to the first and second busses at the end opposite the controller and has a normal state in which the first bus is connected to the second bus thus completing the loop; the shunt may also assume

a state in which each of the first and second serial busses are connected to separate outputs; the separate outputs are used to connect to a new disk array cassis with similar busses and shunting device (**Epsey et al.**, PCT WO 98/21660, May 1998); and

(4) apparatus and method for dynamic reconfiguration of daisy-chained computer mass storage interfaces for improved performance; the system includes a plurality of storage devices and a plurality of control modules in the daisy-chained communication medium; the control modules communicate with the storage devices in redundant controller applications; the controllers communicate amongst one another to coordinate access to the storage devices; the configurations have redundant loops to enhance the reliability of the storage system; the system provides a loop isolation circuit capable of switching states to join or separate two communication loop portions; the loop isolation circuit is inserted into the communication loop to permit one of the two states to be controllably selected: a first state in which the loop is a single continuous loop and a second state wherein the loop is divided into two loop portions; the system enhances the performance by increasing available bandwidth when a large loop is subdivided into two loops (**DeKoning et al.**, U.S. patent 6,055,228).

Additional state of the art reviewed and considered by the Examiner is found in U.S. Patent 6,061,750; U.S. Patent 6,799,224; U.S. Patent 6,289,471; U.S. Patent 5,757,642.

None of these references taken either alone or in combination with the prior art of record discloses a high speed mass storage system which is readily expandable to increase its storage capacity while the system is in operation, specifically including:

(Claim 1) "said first controller providing a communication path between the first server and each said storage device through its associated storage device bypass circuit board and through the module bypass circuit board, said second controller providing a communication path between the second server and each said storage device through its associated storage device bypass circuit board and the module bypass circuit board; and

at least one of said servers being operative to establish direct communication between the first and second controllers, and said first and second controllers being operative to maintain direct communication between the first and second controllers independent of said at least one first computer of said first server and said at least one second computer of said second server".

None of these references taken either alone or in combination with the prior art of record discloses a high speed mass storage system adapted to be readily expandable to increase its capacity while the system is in operation, specifically including:

(Claim 19) "said first controller connecting the at least one first computer of the first controller with each said disk drive through its associated drive bypass circuit board and through the module bypass circuit board such that a loop is formed between the output and input of the first controller with each disk drive bypass circuit board and the module bypass circuit board in said loop and completing said loop whether or not a disk drive is plugged into the disk drive connector; and

said second controller connecting the at least one second computer of the second controller with each said disk drive through its associated drive bypass circuit board and through the module bypass circuit board; and

at least one of said first and second servers being operative to establish direct communication between the first and second controllers, and said first and second controllers being operative to maintain direct communication between the first and second controllers independent of said at least one first computer of said first server and said at least one second computer of said second server".

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez, can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Art Unit 2123
April 12, 2007

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4/14/07